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APPLICANTS

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** CONTINUING DATA *****

This application is a 371 of PCT/SG98/00082 10/13/1998

** FOREIGN APPLICATIONS *****

Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged Examiner's Signature: <i>[Signature]</i> Initials: <i>[Initials]</i>	INDIA	12	10/17	14

ADDRESS

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TITLE

Area efficient realization of coefficient architecture for bit-serial fir, iir filters and combinational/sequential logic structure with zero latency clock output

FILING FEE RECEIVED 1344	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit
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